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Design and Analysis of DSTATCOM and Comparison of Various Control Algorithms

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Abstract: This paper discusses about the three phase three wire distribution static compensator (DSTATCOM) and its performance under various control algorithms. DSTATCOM is a shunt connected advanced power electronic device which provides reactive power compensation, harmonic elimination and source current balancing. It consists of a three phase IGBT inverter module, dc link capacitor, interfacing inductor and the control circuit. Various control algorithms such as Instantaneous Reactive Power Theory (IRPT), Synchronous Reference Frame Theory (SRF), Adaline-based algorithm and Back Propagation control algorithm are compared and its advantage over other are discussed. These control algorithms are used for extracting the reference current signals from the load current to generate the switching pulses for IGBTs of the VSC of the DSTATCOM. Synchronous Reference Frame Theory and Back Propagation control based DSTATCOM are simulated with MATLAB using SIMULINK for various types of loads like linear, nonlinear and unbalanced loads. Linear load used is resistive load and nonlinear load is a three phase diode bridge rectifier feeding a RL load. Simulation results demonstrate the performance of DSTATCOM under these control algorithms

Keywords: DSTATCOM, IRP Theory, SRF Method, Adaline-based control algorithm, Back Propagation Control algorithm.

I. INTRODUCTION

The active and reactive power between sending end and receiving end in an electrical power system should be balanced. If it is not so, the system frequency and voltage unbalance may occur hence power system will become unstable. For stable power system operation, active and reactive control are needed. Distribution Static Var (DSTATCOM) technology is one of the advanced power electronics device which provides fast and continuous capacitive and inductive reactor power compensation. The majority of loads in electrical power system are inductive in nature such as fans and motors etc. These loads draw lagging power factor currents. This excessive reactive power demand increases losses in feeders and reduces the active power flow. Nowadays many industries and utilities faces the voltage sag which is the most important power quality problem. It contributes more than 80% power quality (PQ) problems that exist in power systems. Voltage sag is a reduction in AC voltage at power frequency. It lasts for duration of a half cycles to a few seconds. Voltage sags are very harmful to sensitive loads used in industrial plants such as process controllers, programmable logic controllers (PLC), adjustable speed drives (ASD) and robotics. It has been reported that high intensity discharge lamps used for industrial illumination get extinguished at voltage sags of 20% and industrial equipment's like PLC and ASD are about 10% [1]. Voltage sag affects the system performance. Also when sensitive loads are used, it may initiate significant tripping. Voltage flicker is another power quality problem. It is due to the increase in nonlinear varying loads such as arc furnaces, arc welders, spot welders and shredder motors etc. Many techniques are there to track and extract voltage sags [2].

Distribution Static Compensator (DSTATCOM) has become widely adopted as an efficient voltage sag mitigating device. It has the advantage of optimized energy over DVRs, since the DVRs are mostly connected to the source because the DVR usually injects active and reactive power to restore the load voltage.

Voltage flicker is one of the difficult power quality problems because of its randomness which hinders tracking. Most of the existing extracting techniques depend on the FFT and its derivatives. The traditional mitigating device is Static VAR Compensator (SVC) which mitigate flicker produced by arc furnaces. The DSTATCOM gives a much better performance than the SVC [3]-[5]. The control techniques are Instantaneous reactive power theory [6], Synchronous reference frame theory [6], Adaline based neural network [7] and Back Propagation control [8].

In this paper, various control algorithm used for the control of a DSTATCOM is analysed and the performance of a DSTATCOM is studied through design and simulation.

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II. DESIGN OF DSTATCOM

DSTATCOM is used to generate or absorb reactive power. The DSTATCOM is a three-phase shunt connected power electronics based device. It is connected near the load . It consists of a dc capacitor, three-phase inverter (IGBT, thyristor), ac filter, coupling transformer and a control circuit as shown in figure 1. The important part of the DSTATCOM is the voltage source inverter that converts an input dc voltage into a three phase output voltage at fundamental frequency. The controller of the D-STATCOM is used to operate the inverter in such a way that the phase angle between the inverter voltage and the line voltage is dynamically adjusted so that the D-STATCOM generates or absorbs the desired reactive power at the Point of common coupling(PCC). If output voltage of the inverter is equal to system

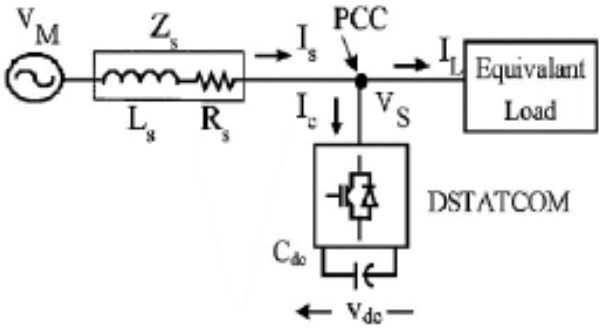

Fig 1: Single-line diagram of DSTATCOM system

voltage Vs, the reactive power is zero and the D-STATCOM does not generate or absorb reactive power. When inverter voltage is greater than system voltage, the current Ic, flows through the coupling inductor from the D-STATCOM to the ac system, which means DSTATCOM injects the current to the system and the device generates capacitive reactive power. If the inverter voltage is less than system voltage, the current flows from the ac system to the DSTATCOM, resulting in the device absorbing inductive reactive power. A three-phase voltage source converter (VSC) is realized using six IGBTs switches with anti-parallel diodes. Three phase loads may be a lagging power factor load or an unbalance load or a nonlinear load. A filter is connected to the system in parallel with the load and the compensator to reduce switching ripples in the PCC voltage injected by switching of DSTATCOM. The DSTATCOM can be used for reactive power compensation for power factor correction or voltage regulation [9]-[10].

A DSTATCOM is a shunt connected power electronic based device which is used in an AC distribution system where, harmonic current mitigation, reactive current compensation and load balancing are necessary. DSTATCOM consists of a voltage source converter (VSC) which has self-commutating semiconductor valves and a capacitor on the DC bus. The device is shunt connected to the distribution network through a coupling inductance. In general, the DSTATCOM can provide power factor correction, harmonics compensation and load balancing. The major advantages of DSTATCOM include the ability to generate the rated current at virtually any network voltage, better dynamic response and the use of a relatively small capacitor on the DC bus.

Fig. 2 shows the schematic diagram of a DSTATCOM connected to a three phase AC mains feeding three phase loads, such as lagging power factor loads or unbalanced loads or non-linear loads or mixed of these loads. Interfacing inductors (Lf) are used at AC side of the voltage source converter (VSC) for reducing ripple in compensating currents. Ripple filter consists of a small series connected capacitor (Cf) and resistor (Rf), and is installed at PCC in parallel with the loads and the compensator to filter out the high frequency switching noise of the voltage at PCC. DSTATCOM injects harmonics/reactive currents to cancel the harmonics /reactive power component of the load currents. Hence the source currents are harmonic free and load reactive power is also compensated. The voltage and current rating of the required compensation decides the rating of the switches.

The selection of the DC bus voltage, DC bus capacitor, AC inductors in the following sections and the obtained values are shown in appendix and the ripple filter of DSTATCOM are given in,

A. DC Capacitor Voltage

The value of DC bus voltage (Vdc) depends on the PCC voltage and its must be greater than amplitude of the AC mains voltage for successful PWM control of VSC of DSTATCOM. For a three-phase VSC, the DC bus voltage is defined as,

$$V_{dc} = 2\sqrt{2}V_{LL} / (\sqrt{3}m) \quad (1)$$

where, m is the modulation index and is considered as 1 and VLL is the AC line output voltage of DSTATCOM.

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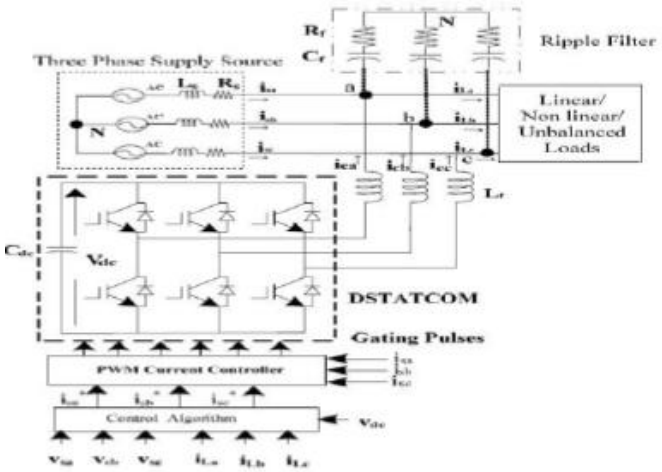

Fig 2: Schematic Diagram of DSTATCOM

B. DC Bus Capacitor

The design of the DC bus capacitor is governed by the depression in the DC bus voltage upon the application of the loads and rise in the DC bus voltage on removal of the loads. Using the principle of energy conservation, the equation governing Cdc is as,

$$0.5Cdc\,[(V\ 2dc) - (V\ 2dc1)] = 3V\ (aI)\ t \qquad (2)$$

where, Vdc is the nominal DC voltage and Vdc1 is the minimum voltage level of DC bus, a is the over loading factor, Vph is the phase voltage, I is the phase current of the VSC and t is time for which DC bus voltage is to be recovered and a1 is the safety factor has a value is taken as 1.5.

C. AC Inductor

The selection of the AC inductance depends on the ripple current, icr,(p-p) and switching frequency fs, The AC inductance is given as,

$$Lf = \sqrt{3}mVdc/(12 * a * fs * icr, (p\text{-}p)) \qquad (3)$$

switching frequency (fs), modulation index (m), DC bus voltage (Vdc), over load factor(a) AC inductance (Lf). The current ripple is taken as 1%.

D. Ripple Filter

A first order high pass filter tuned at half of the switching frequency is used to filter the high frequency noise from the voltage at the point of common coupling. A capacitor with series resistance is selected as a ripple filter. This filter orders high impedance at fundamental frequency and low impendence at half of the switching frequency which prevents the flow of fundamental components at fundamental frequency in the ripple filter branch and allows the flow of high frequency noises through the ripple filter branch at higher than fundamental frequency [4]-[5], [11].

III. COMPARISON OF CONTROL ALGORITHMS

The performance of DSTATCOM depends on the control algorithm used for extraction of reference current components. Many control schemes are used for the controlling purpose, and some of these are instantaneous reactive power (IRP) theory, instantaneous symmetrical components, synchronous reference frame (SRF) theory, current compensation using dc bus regulation, computation based on per phase basis, and scheme based on neural network techniques. Among these control schemes, IRP and SRF theories are most widely used.

A. Instantaneous Reactive Power Theory

Instantaneous Reactive Power theory was initially proposed by Akagi [6]. This theory is based on the transformation of three-phase quantities to two-phase quantities in α-β frame and the calculation of instantaneous active and reactive power in this frame.

A basic block diagram of this technology is shown in Fig. 3. Sensed inputs Va, Vb , and Vc and iLa, iLb, and iLc are fed to the controller, and these quantities are processed to generate reference current commands (i*sa, i*sb, and i*sc), which are fed to a hysteresis-based pulse width modulated (PWM) signal generator to generate signal switching signals fed to the DSTATCOM.

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B. Synchronous Reference Frame Method

SRF theory is based on the transformation of currents in synchronously rotating dq frame [6]. Fig.3 shows the basic building blocks of this theory. Sensed inputs Va, Vb, and Vc and iLa, iLb, and iLc are fed to the controller. Voltage signals are processed by a phase-locked loop (PLL) to generate unit voltage templates (sine and cosine signals) [12]. Current signals are transformed to dq frame, where these signals are filtered and transformed back to abc frame (isa, isb, and isc), which are fed to a hysteresis-based PWM signal generator to generate signal switching signals fed to the DSTATCOM.

Similar to the pq theory, current components in coordinates are generated, and using as a transformation angle, these currents are transformed from to dq frame defined as (Parks transformation). SRF isolator extracts the dc component by low-pass filters (LPFs). The extracted dc components id,dc and iq,dc are transformed back into αβ frame using reverse Parks transformation. From these currents, the transformation is made to obtain three-phase reference source currents in abc coordinates. Reactive power compensation can also be provided by keeping iq component zero for calculating the reference source currents [6], [9].

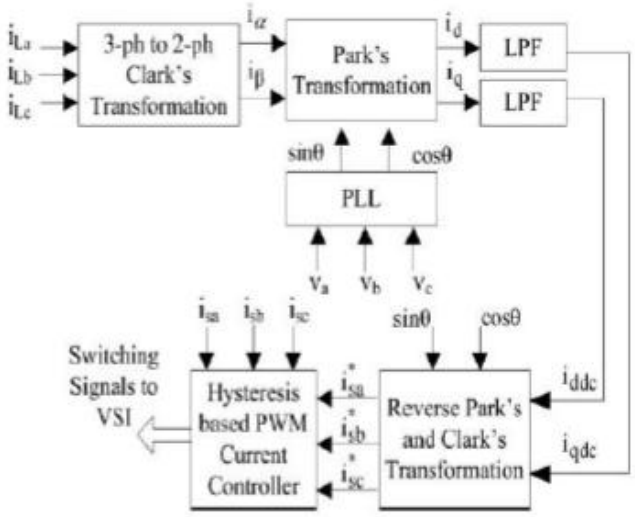

Fig 3: Block diagram of the control algorithm using Synchronous Reference Frame Method.

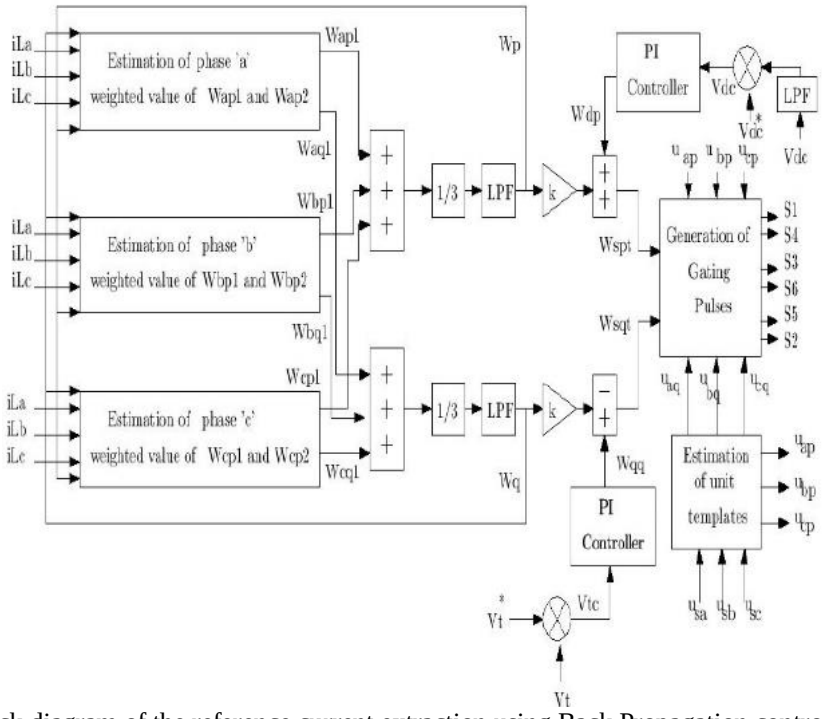

Fig 4: Block diagram of the reference current extraction using Back Propagation control algorithm

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C. Adaline-Based Control Algorithm

The basic theory of the Adaline decomposer has been based on LMS algorithm and its training through Adaline, which tracks the unit vector templates to maintain minimum error. The basic concept of theory used here can be understood by considering the analysis in single-phase system. The control algorithm is based on the extraction of current component in phase with the unit voltage template. To estimate the fundamental frequency positive sequence real component of load current, the unit voltage template should be in phase with the system voltage and should have unit amplitude, and it must be undistorted. For the calculation of templates, voltage at the point of common coupling is sensed. Sensed voltages are filtered through a band pass filter, and their amplitude is computed. Sensed three-phase voltages are divided by this amplitude to get three-phase voltage templates (ua, ub, and uc). The weight is a variable and changes as per the load current and magnitude of phase voltage. This scheme for estimating weights corresponding to the fundamental frequency real component of current (for three-phase system), based on LMS-algorithm-tuned Adaline, tracks the unit voltage templates to maintain minimum error. Three-phase reference source currents corresponding to positive sequence real component of load current computed using this weight. Currents are fed to the hysteresis-based PWM current controller to control the source currents to follow the reference source currents in UPF mode of operation. These currents are considered as the reference source currents iref (i*sa, i*sb, and i*sc), and along with the sensed source currents iact (isa, isb, and isc), these currents are fed to a hysteresis-based PWM current controller to control the source currents to follow these reference currents. Switching signals generated by PWM current controller control the source currents close to the reference current. Switching signals are generated on the following logic, where hb is the hysteresis band around the reference current iref [6]-[7].

D. Back-Propagation Control Algorithm

Fig. 4 shows the block diagram of the BP training algorithm for the estimation of reference source currents through the weighted value of load active power and reactive power current components. In this algorithm, the phase PCC voltages (Vsa, Vsb, and Vsc), source currents (isa, isb, and isc), load currents (iLa, iLb, and iLc) and dc bus voltage (Vdc) are required for the extraction of reference source currents (i* sa, i*sb, and i*sc). There are two primary modes for the operation of this algorithm: The first one is a feed forward, and the second is the BP of error or supervised learning [8].

IV. SIMULATION OF DSTATCOM

The parameters are given in appendix. The basic simulation model consists of a source, load, DSTATCOM and control block. The linear load connected is a combination of resistance and inductance in series for each phase and the nonlinear load is a diode bridge rectifier. This DSTATCOM is simulated with the above described Synchronous Reference Frame theory and and new back propagation control algorithm.

A. Synchronous Reference Frame Control

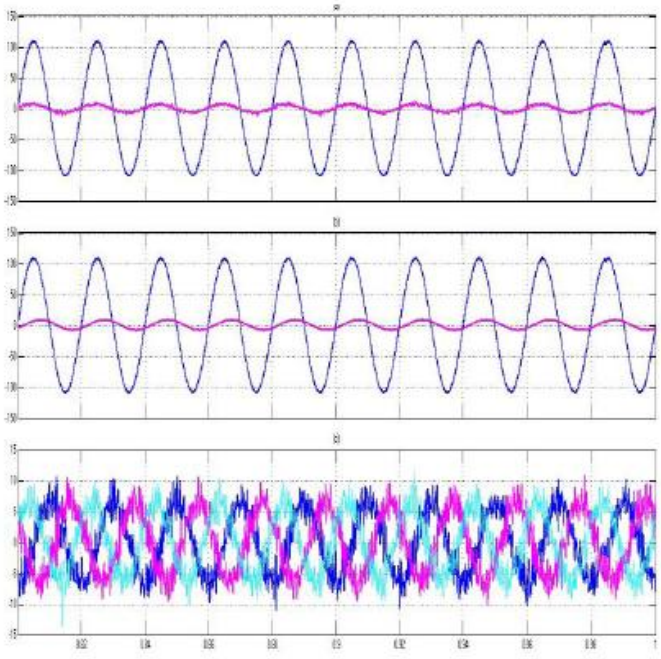

Fig 5: the waveforms of (a) Source voltage and source current (b) Source voltage and Load current (c) DSTATCOM current for linear load

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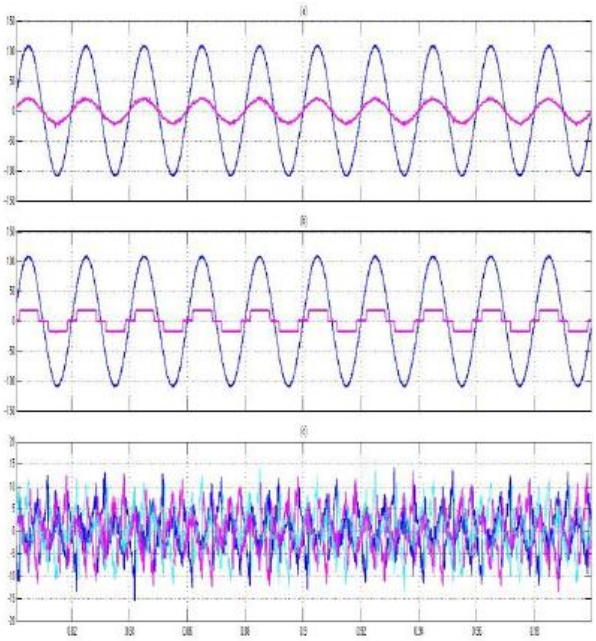

Fig 6: the waveforms of (a) Source voltage and source current (b) Source voltage and Load current (c) DSTATCOM current for nonlinear load.

Fig 5 (a) and (b) shows the waveforms of source voltage, source current and load current for linear loads when Synchronous Reference Frame Theory is used. From this waveforms we can see that the source voltage and source current are in phase with each other and load current lags behind source voltage. Fig 5(c) shows the waveform of DSTATCOM current. Fig 6 (a) and (b) shows the waveforms of source voltage, source current and load current for nonlinear loads. Here source voltage and source current are in phase and load current lags behind the source voltage. For both loads, the magnitude of load current is less than the source current. Fig 6 (c) shows the waveform of DSTATCOM current. Due to the presence bridge rectifier, harmonics are injected in the system. These harmonic current is injected by DSTATCOM and harmonics can be successfully eliminated and source current can be made

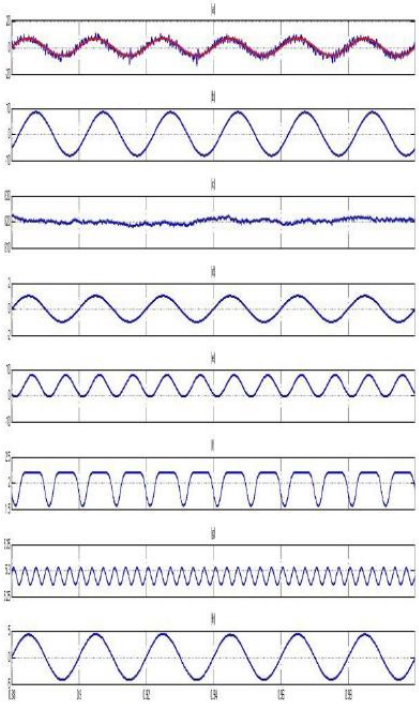

Fig 7: Waveforms generated using BP algorithm (a) Source voltage and Source current (b) Load current (c) dc bus voltage (d), (e), (f) are extracted currents at different stages of control algorithm (g) weighted value of extracted current (h) reference current for linear load almost sinusoidal. Also power factor is made unity.

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B. Back Propagation (BP) Control

Fig 7 shows the waveforms of (a) source voltage and source current (b) Load current (c) DC bus voltage (d),(e),(f),(g) are extracted stages of control algorithm and (h) Reference current for linear loads when Back Propagation control is used. From this waveforms we can see that the source voltage and source current are in phase with each other and load Current lags behind source voltage after DSTATCOM is switched on at 0.1 second. Fig 8 shows the waveforms of (a) source voltage and source current, (b) load current (c) dc

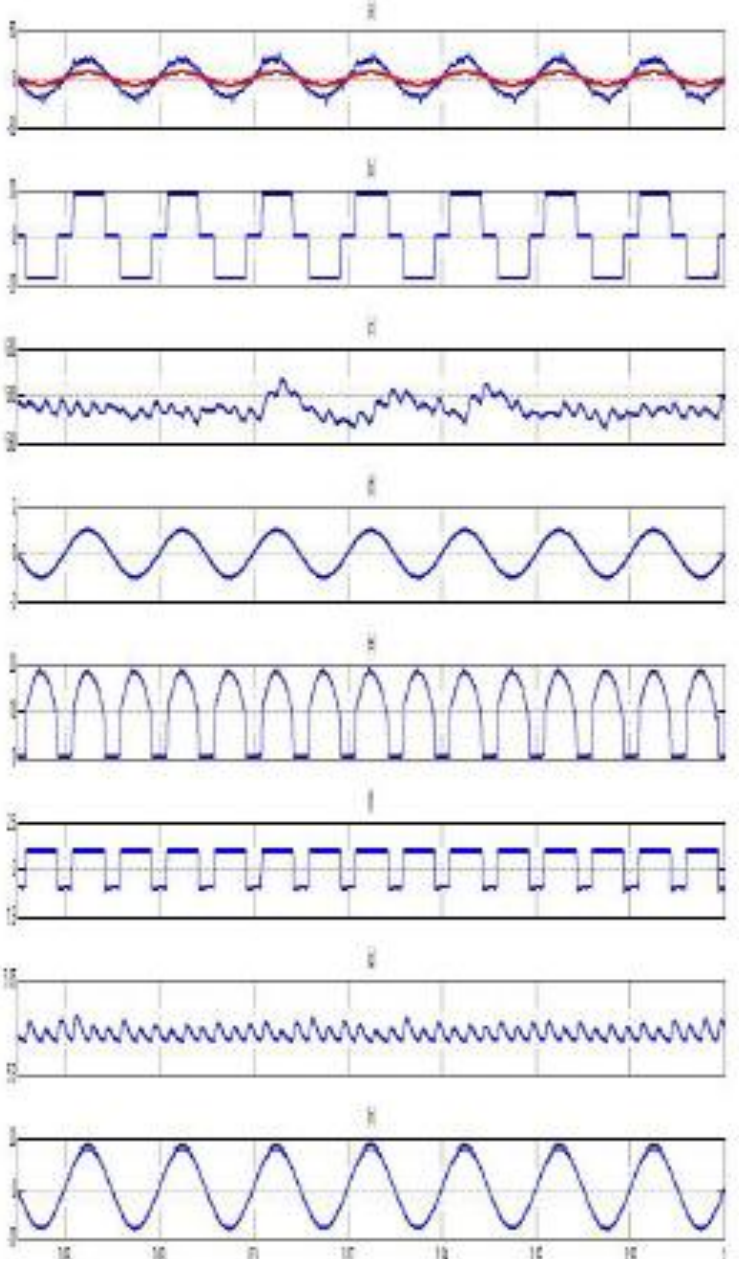

Fig 8: Waveforms generated using BP algorithm (a) Source voltage and Source current (b) Load current (c) dc bus voltage (d), (e), (f) are extracted currents at different stages of control algorithm (g) weighted value of extracted current (h) reference current for nonlinear load.

bus voltage, (d),(e),(f),(g) are extracted currents at different stages of control algorithm and (h)reference current for nonlinear loads when Back Propagation control is used. Here source voltage and source current are in phase and load current lags behind the source voltage when DSTATCOM is included in the circuit. For both loads, the magnitude of load current is less than the source current. Due to the presence bridge rectifier, harmonics are injected in the system. These harmonic current is injected by DSTATCOM and harmonics can be successfully eliminated and source current can be made almost sinusoidal. Also power factor is made unity. Hence reactive power compensation and harmonic compensation took place.

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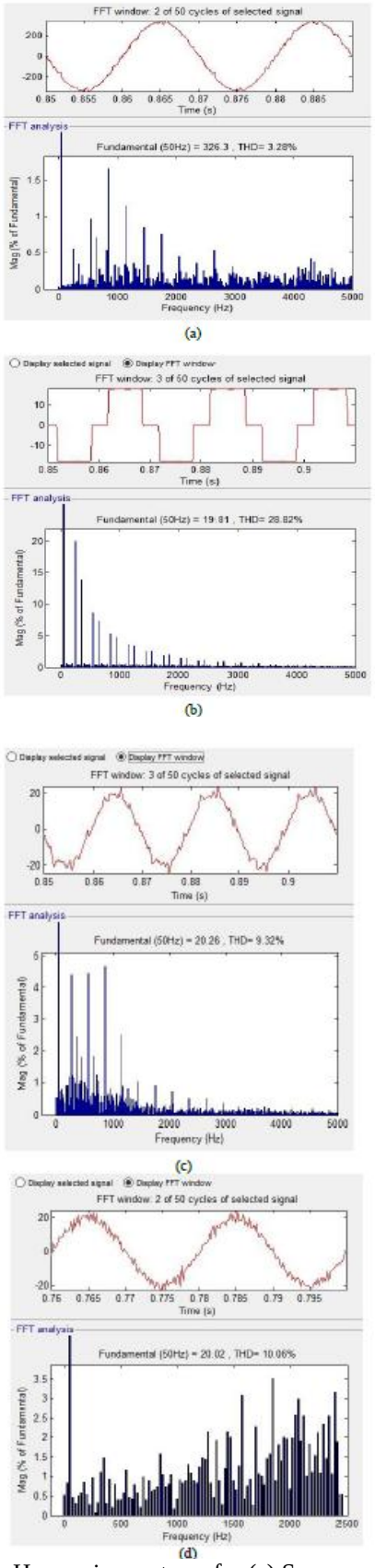

Fig 9: Harmonic spectrum for (a) Source voltage
(b) Load current (c) Source current for Back Propagation control (d) Source current for Synchronous Reference Frame Theory.

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Fig 9 shows the waveforms and harmonic spectrum of source voltage, load current and source current for Back Propagation control and Synchronous reference frame control for nonlinear load. It shows the source voltage and load current having the THD of 3.28% and 28.82% respectively. The source current having THD of 10.06% when Synchronous Reference Frame Theory is used and 9.32% when Back Propagation control is used.

V. CONCLUSION

In this paper, various control algorithms for a three phase three wire DSTATCOM for power quality improvement are discussed. The main purpose of this DSTATCOM is to compensate reactive, harmonic load and to balance the source currents. The various control algorithms are instantaneous reactive power (IRP) theory, instantaneous symmetrical components, synchronous reference frame (SRF) theory, Adaline based control algorithm and Back-Propagation Control Algorithm. DSTATCOM provides reactive power required by the load and therefore the source current remains at unity power factor. Hence only real power is being supplied by source. Back propagation control algorithm has been used for the extraction of the reference source currents to generate the switching pulses for IGBTs of the VSC of the DSTATCOM and performance of DSTATCOM is analysed through design and simulation. The results show that the source voltage and load current having the THD of 3.28% and 28.82% respectively. The source current having THD of 10.06% when Synchronous Reference Frame Theory is used and 9.32% when Back Propagation control is used. THD is of the source current is less in Back Propagation based DSTATCOM.

APPENDIX

Line impedence: Rs: 0.01Ω, Ls: 2 mH
AC line voltage: 415 V, 50 Hz
DC voltage PI controller: Kpd = 0.025, Kid =0.14
Loads:

1. Linear: R=100Ω
2. Nonlinear: three phase bridge rectifier with R=100Ω.

DC bus voltage of DSTATCOM: 820 V
DC bus capacitance of DSTATCOM: 500 μF

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